

# DESIGN OF SNUBBERS FOR POWER CIRCUITS

By Rudy Severns

## What's a snubber?

Power semiconductors are the heart of power electronics equipment. Snubbers are circuits which are placed across semiconductor devices for protection and to improve performance. Snubbers can do many things:

- Reduce or eliminate voltage or current spikes
- Limit  $dI/dt$  or  $dV/dt$
- Shape the load line to keep it within the safe operating area (SOA)
- Transfer power dissipation from the switch to a resistor or a useful load
- Reduce total losses due to switching
- Reduce EMI by damping voltage and current ringing

There are many different kinds of snubbers but the two most common ones are the resistor-capacitor (RC) damping network and the resistor-capacitor-diode (RCD) turn-off snubber. This application note will show you how to design these two snubbers.

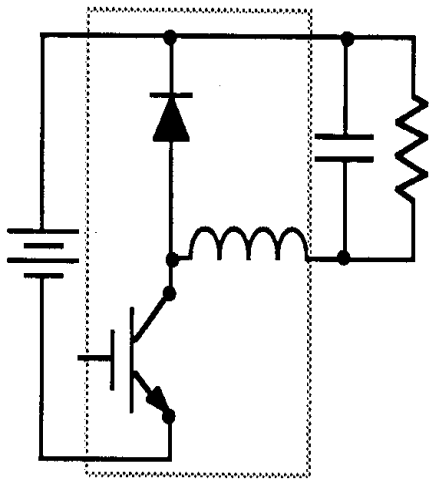
## Switching waveforms

Before getting into the design of snubbers it is important to understand the waveforms which occur naturally in power circuits. These provide both the motivation for using snubbers and the information needed for their design. There are many different types of circuits used in power converters, motor drives, lamp ballasts and other devices. Fortunately all of these different circuits have a common network and waveforms associated with the switches. Figure 1 shows four widely used circuits. All of these circuits, and in fact most power electronics circuits, have within them the same switch-diode-inductor network shown within the dotted lines. The behavior of this network is the same in all these circuits which means that we only have to solve the snubber design problem for one circuit to apply it to all of the others. This tremendously simplifies the problem and allows generalized snubber design techniques.

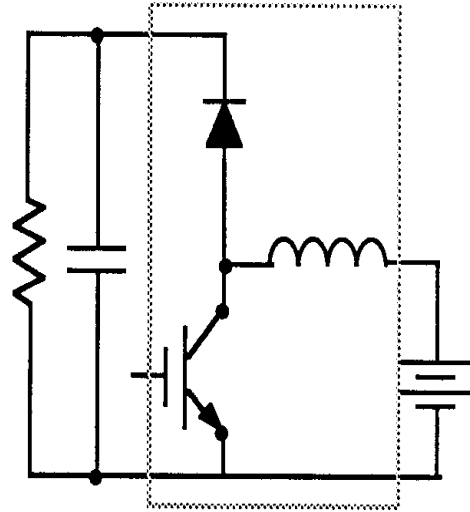
A typical boost converter is shown in figure 2A. For snubber design we are concerned with circuit behavior during the switch transition time which is much shorter than the switching period. This allows us to simplify the analysis. In normal operation the output voltage is DC with very little ripple. This means that we can replace the load and filter capacitor with a battery since the output voltage changes very little during switch transitions. The current in the inductor will also change very little during a transition and we can replace the inductor with a current source. The simplified circuit is given in figure 2B. The voltage (E) and current (I) waveforms are given in figure 2C.

At the beginning of the switching cycle the switch is open and all of the current ( $I_0$ ) will be flowing through the diode into the battery. As the switch turns on, the current will gradually shift from the diode to the switch. However, as long as there is

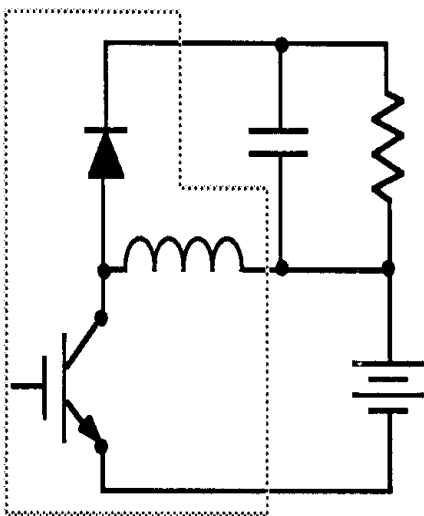
# Figure 1



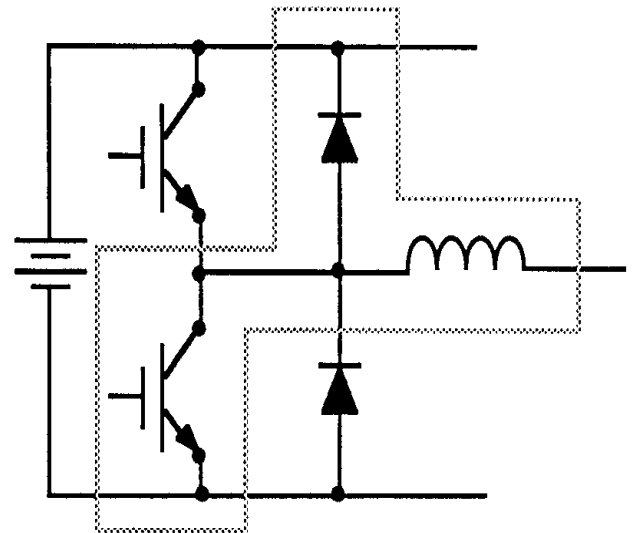
Buck



Boost



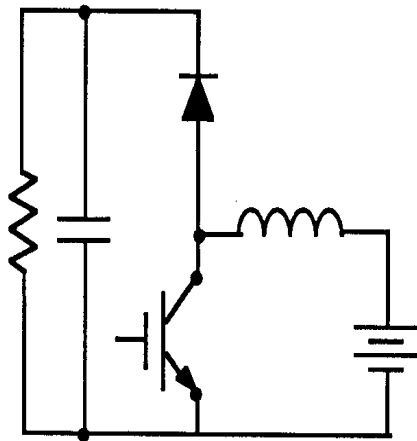
Buck-Boost



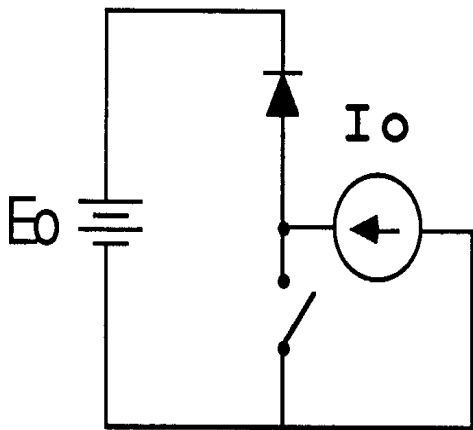
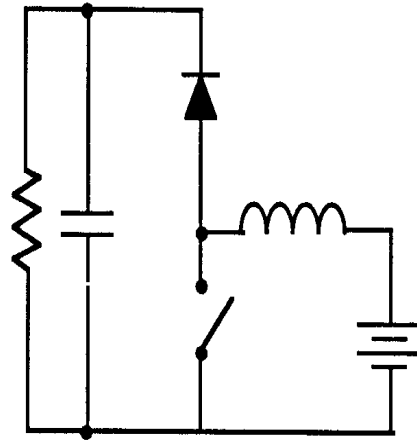
Inverter Pole

# Figure 2

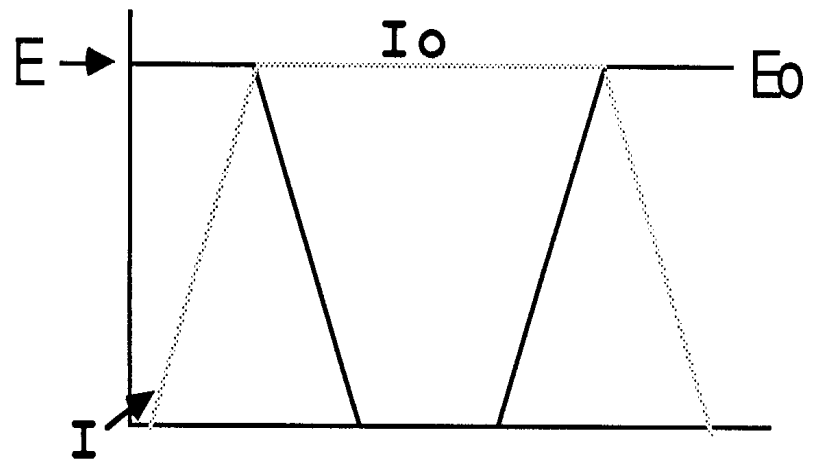
## Boost Converter



(a)



(b)



(c)

current in the diode, the switch voltage will remain at  $E_o$ . Once all of the current has been transferred to the switch, the switch voltage can begin to fall. At turn-off the situation is reversed. As the switch turns off, the voltage across it will rise. The current in the switch will however, not begin to fall until the switch voltage reaches  $E_o$  because the diode will be reverse biased until that point. Once the diode begins to conduct the current in the switch can fall.

This type of switching, commonly referred to as “hard switching”, exposes the switch to high stress because the maximum voltage and maximum current must be supported simultaneously. This also leads to high switching loss.

In practical circuits the switch stress will be even higher due to the unavoidable presence of parasitic inductance ( $L_p$ ) and capacitance ( $C_s$ ) as shown in figure 3A.  $C_p$  includes the junction capacitance of the switch and stray capacitance due to circuit layout and mounting.  $L_p$  is due to the finite size of the circuit layout and lead inductance.  $L_p$  can be minimized with good layout practice but there may be some residual inductance which may cause a ringing voltage spike at turn-off as shown in figure 3B.

The most common reasons for using a snubber are to limit the peak voltage across the switch and to reduce the switching loss during turn-off.

### RC snubber design

An RC snubber, placed across the switch as shown in figure 4, can be used to reduce the peak voltage at turn-off and to damp the ringing. In most cases a very simple design technique can be used to determine suitable values for the snubber components ( $R_s$  and  $C_s$ ). In those cases where a more optimum design is needed, a somewhat more complex procedure is used.

Quick snubber design: To achieve significant damping  $C_s > C_p$ . A good first choice is to make  $C_s$  equal to twice the sum of the output capacitance of the switch and the estimated mounting capacitance.  $R_s$  is selected so that  $R_s = E_o / I_o$ . This means that the initial voltage step due to the current flowing in  $R_s$  is no greater than the clamped output voltage. The power dissipated in  $R_s$  can be estimated from peak energy stored in  $C_s$ :

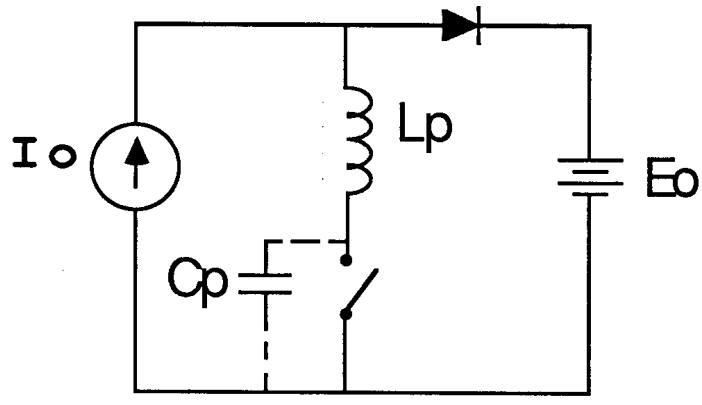
$$U_p = \frac{C_s E_o^2}{2}$$

This is the amount of energy dissipated in  $R_s$  when  $C_s$  is charged and discharged so that the average power dissipation at a given switching frequency ( $f_s$ ) is:

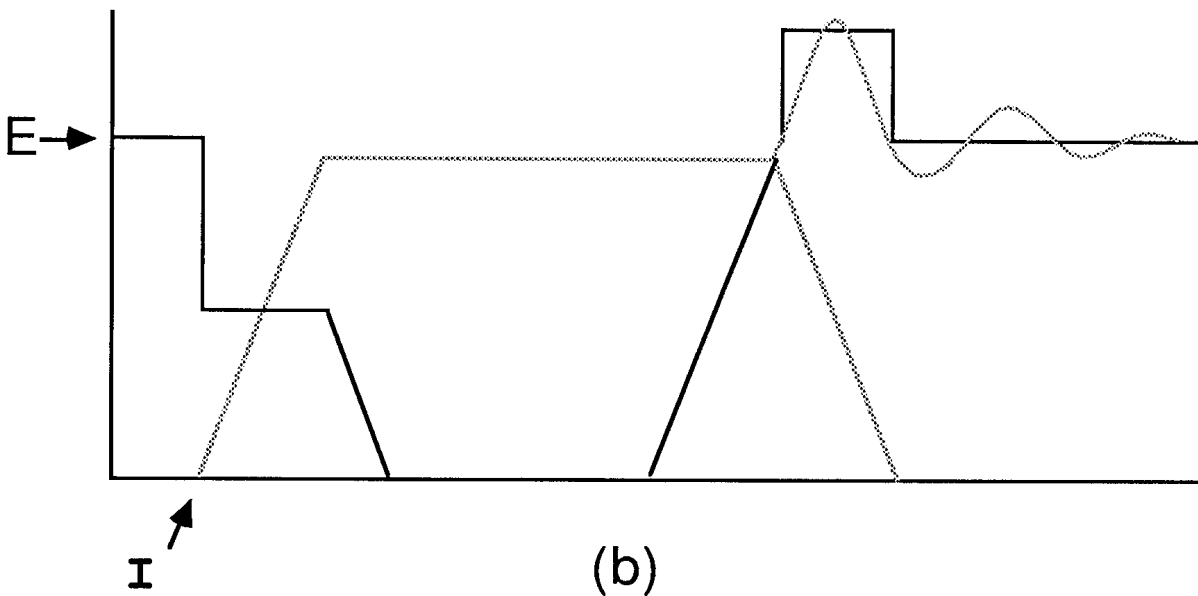
$$P_{diss} \approx C_s E_o^2 f_s$$

Depending on the amount of ringing the actual power dissipation will be slightly higher than this.

# Figure 3

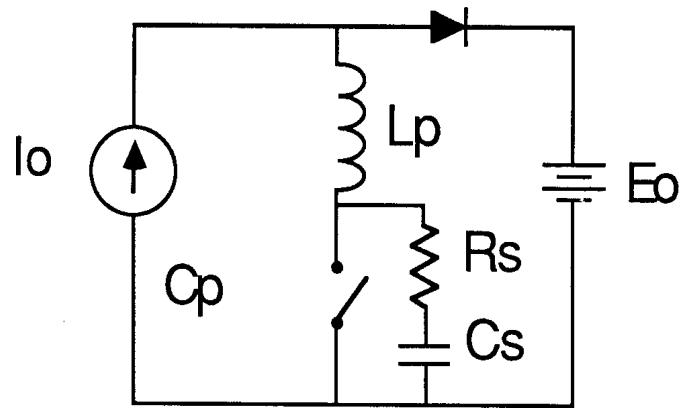


(a)



(b)

**Figure 4**



The following example shows how to use this procedure. Suppose the switch is an IRF740 with  $I_o = 5$  A and  $E_o = 160$  V. For this device  $C_{oss} = 170$  pF and the mounting capacitance will be 40 pF. Doubling this capacitance,  $C_s = 420$  pF. A 500V Snubber Mike capacitor would be ideal for this application and the standard values available are 390 and 470 pF. We will choose the closest standard value and set  $C_s = 390$  pF.  $R_s = E_o/I_o = 32\Omega$ . For  $f_s = 100$  kHz,  $P_{diss} = 1$ W. A 2 Watt carbon composition resistor would be ideal for  $R_s$  because it has very low self inductance. Carbon film resistors can also be used as long as those resistors which are trimmed with a spiral cut are avoided.

If this very simple and practical procedure does not limit the peak voltage sufficiently then  $C_s$  can be increased or the optimizing procedure can be used.

Optimized RC snubber: In those cases where the peak voltage must be minimized and power dissipation is critical, a more optimum design approach should be used. In a classic paper [1] Dr. W. McMurray described the optimization of the RC snubber. The following discussion presents the highlights of the procedure.

The following definitions will be used:

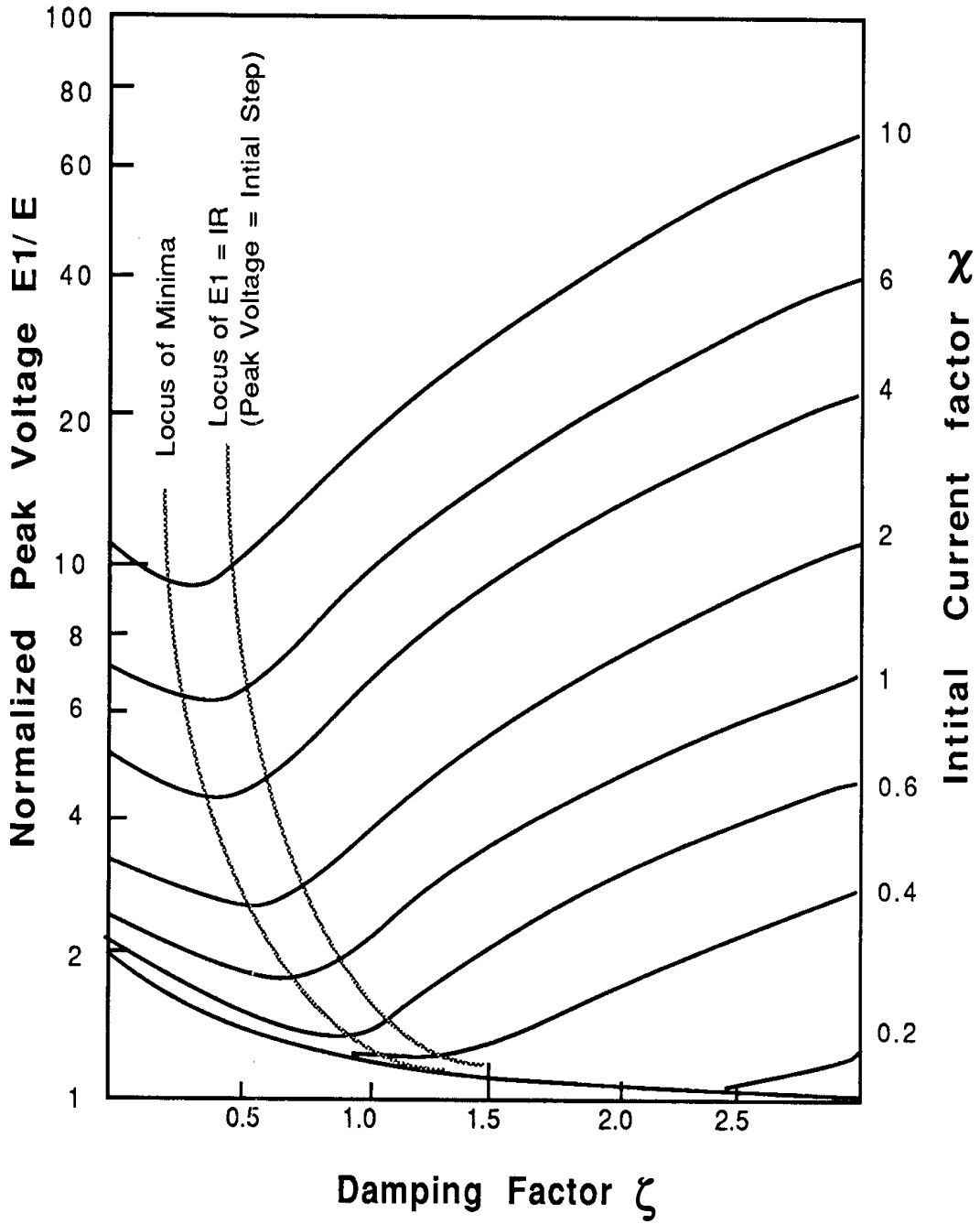
$Z_o = (L_p/C_s)^{1/2}$	
$\chi = (I_o/E_o)Z_o$	initial current factor
$\chi^2 = L_p I_o^2 / C_s E_o^2$	initial energy in $L_p$ /final energy in $C_s$
$\zeta = P_s/2Z_o$	damping factor
$E_1 =$	peak switch voltage
$E_1/E_o =$	normalized peak switch voltage

In the design process  $I_o$ ,  $E_o$  and  $L_p$  will be given and it will be necessary to determine the values for  $R_s$  and  $C_s$  which give an acceptable peak voltage ( $E_1$ ). Figure 5 shows the relationship between  $E_1/E_o$  and  $\zeta$  for different values of  $\chi$ . The key point which this graph makes is that for a given  $\chi$  ( $\chi \propto 1/C_s$ ) there is an optimum value for  $\zeta$  ( $\zeta \propto R_s$ ) which gives the lowest peak voltage. A second important point is that the lowest value of peak voltage attainable is determined by the size of  $C_s$ . If a lower peak voltage is required, then a larger  $C_s$  must be used. This means that the power dissipation has to increase as the peak voltage is reduced.

The design of an optimized RC snubber is very easy using the graph given in figure 6. The design proceeds in the following steps:

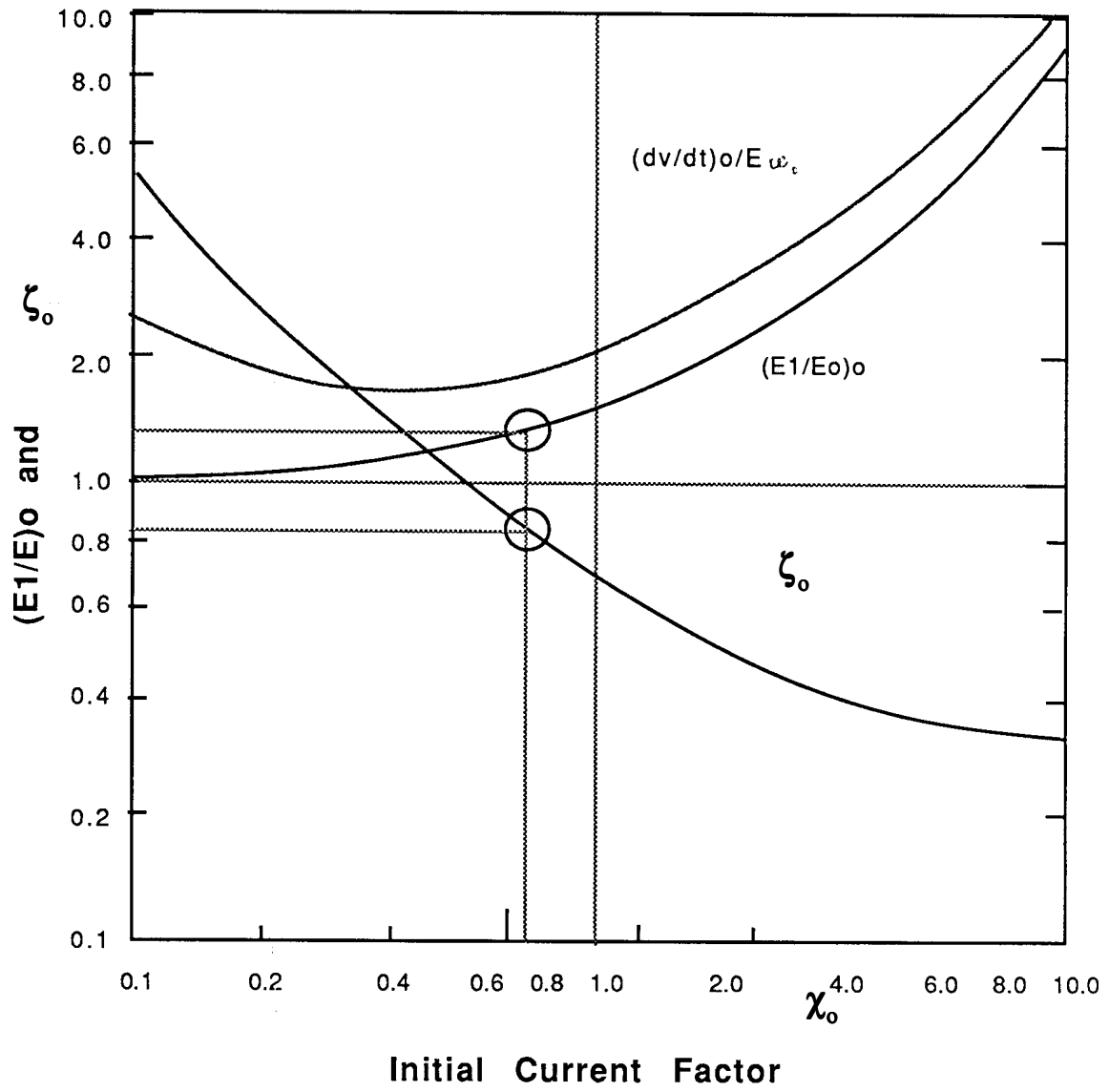
1. Determine  $I_o$ ,  $E_o$  and  $L_p$
2. Select the maximum peak voltage

# Figure 5





# Figure 6



3. Compute  $E_1/E_0$
4. From the graph, determine the values for  $\chi$  and  $\zeta$
5. Given  $\chi$  and  $\zeta$  calculate the values for  $R_s$  and  $C_s$

Here is an actual example. If  $I_0 = 5$  A,  $E_0 = 300$  V,  $L_p = 1\mu\text{H}$  and  $E_1 = 400\text{V}$  then  $E_1/E_0 = 1.33$ . Following the dashed line and arrows on figure 6,  $\chi_0 = 0.65$  and  $\zeta_0 = .8$ . From this information  $R_s$  and  $C_s$  can be determined:

$$C = \left(\frac{I_0}{E_0}\right)^2 \left(\frac{L_p}{\chi_0^2}\right) = 657\text{pF}$$

$$R_s = 2\zeta_0 \sqrt{\frac{L_p}{C_s}} = 614\Omega$$

using a standard CDE “Snubber Mike” capacitor let  $C_s = 680\text{pF}$   
 using a standard resistor let  $R_s = 62$  Ohms

The graphs (figures 5 and 6) do not take into account the effect of the switch shunt capacitance or finite transition time. In general the optimum value for  $R_s$  will be somewhat lower than calculated. A more precise optimum can be achieved by simulation of the switching with SPICE. Starting with the computed values,  $R_s$  can then be easily varied to find the optimum. In general the optimum will be quite broad allowing the use of standard 5% resistor values.

An example of optimizing  $R_s$ , using an IRF840 for the switch, is shown in figure 7. The optimum value for  $R_s = 51$  Watts and  $E_1 = 363$  V. For  $R_s = 39$  and  $62$  Watts,  $E_1$  is higher. The final peak voltage is less than  $400$  V because of the shunt capacitance of the switch. If  $E_1$  is allowed to rise to  $400$  V then a smaller value for  $C_s$  could be used, saving some power dissipation.

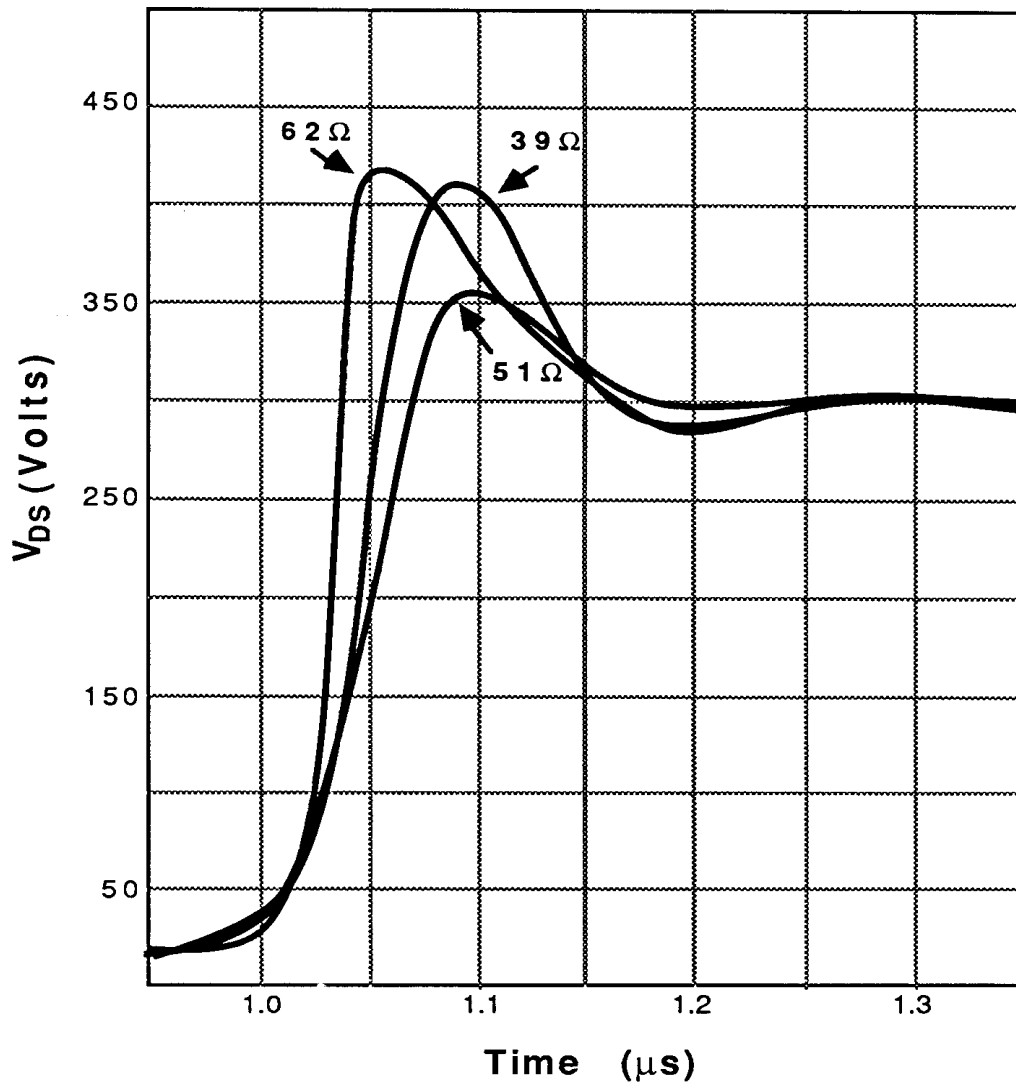
This example shows the importance of simulating and optimizing the snubber circuit using the actual components. The graphs get you into the ball park and the simulation allows for optimization.

### **Determination of $L_p$ :**

$E_0$  and  $I_0$  come directly from the circuit. The value for  $E_1$  is a judgment call and will depend on the voltage rating of the switch and the voltage derating factor. The designer must choose the peak acceptable voltage. All of these quantities are fairly obvious.  $L_p$  however, is a characteristic of the particular circuit layout and is not usually easy to calculate.  $L_p$  can be determined from the circuit by measuring the period of one ringing cycle ( $T_1$ ), then adding a known capacitor ( $C_{\text{test}}$ ) in parallel with the switch and finally re-measuring the period ( $T_2$ ).  $L_p$  can be computed from:

$$L_p = (T_2^2 - T_1^2) \left( \frac{1}{4\pi^2 C_{\text{test}}} \right)$$

# Figure 7



Usually  $C_{test}$  is approximately equal to twice the switch capacitance

An alternate method for determining  $L_p$  in higher power circuits is to take advantage of the voltage step ( $V_{step}$ ) which appears in  $V_{ce}$  or  $V_{ds}$  due to the  $di/dt$  of the current flowing in  $L_p$  at turn-on:

$$L = \left( \frac{V_{step}}{di/dt} \right)$$

At switch turn-on  $C_s$  will be charged. This means that there will be a current spike in the switch due to the discharge of  $C_s$  through  $R_s$  in addition to the normal current flow. This is a short transient pulse which rapidly decays but it can add substantially to the turn-on current and should be taken into account. It should be noted that the RCD snubber discussed in the next section will also have this turn-on current spike but that spike can be controlled more easily because the value for  $R_s$  does not have to be optimized for maximum damping.

RC snubbers are very useful for low and medium power applications but when the power level is more than a few hundred watts the loss in the snubber can be excessive and other types of snubbers need to be considered. The RC snubber does have a place in high power applications as a secondary damping network to suppress high frequency ringing which does not have a lot of energy associated with it.

### **RCD snubber design**

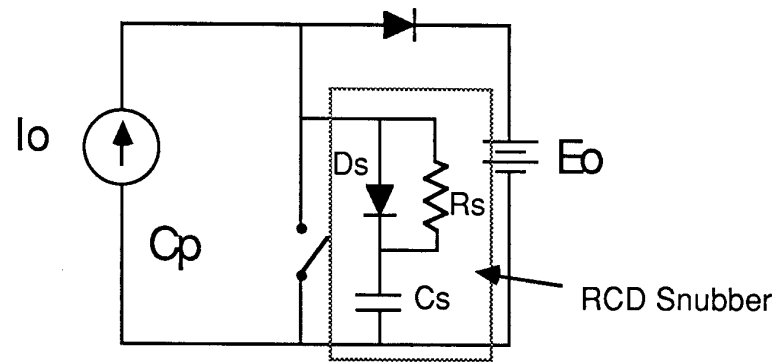
The RCD snubber as shown in figure 8 has several advantages over the RC snubber:

- In addition to peak voltage limiting, the circuit can reduce the total circuit loss, including both switching and snubber losses.
- Much better load lines can be achieved, allowing the load line to pass well within the SOA.
- For a given value of  $C_s$ , the total losses will be less
- The shunt capacitance across the switch ( $C_p$ ) is a useful part of the snubber

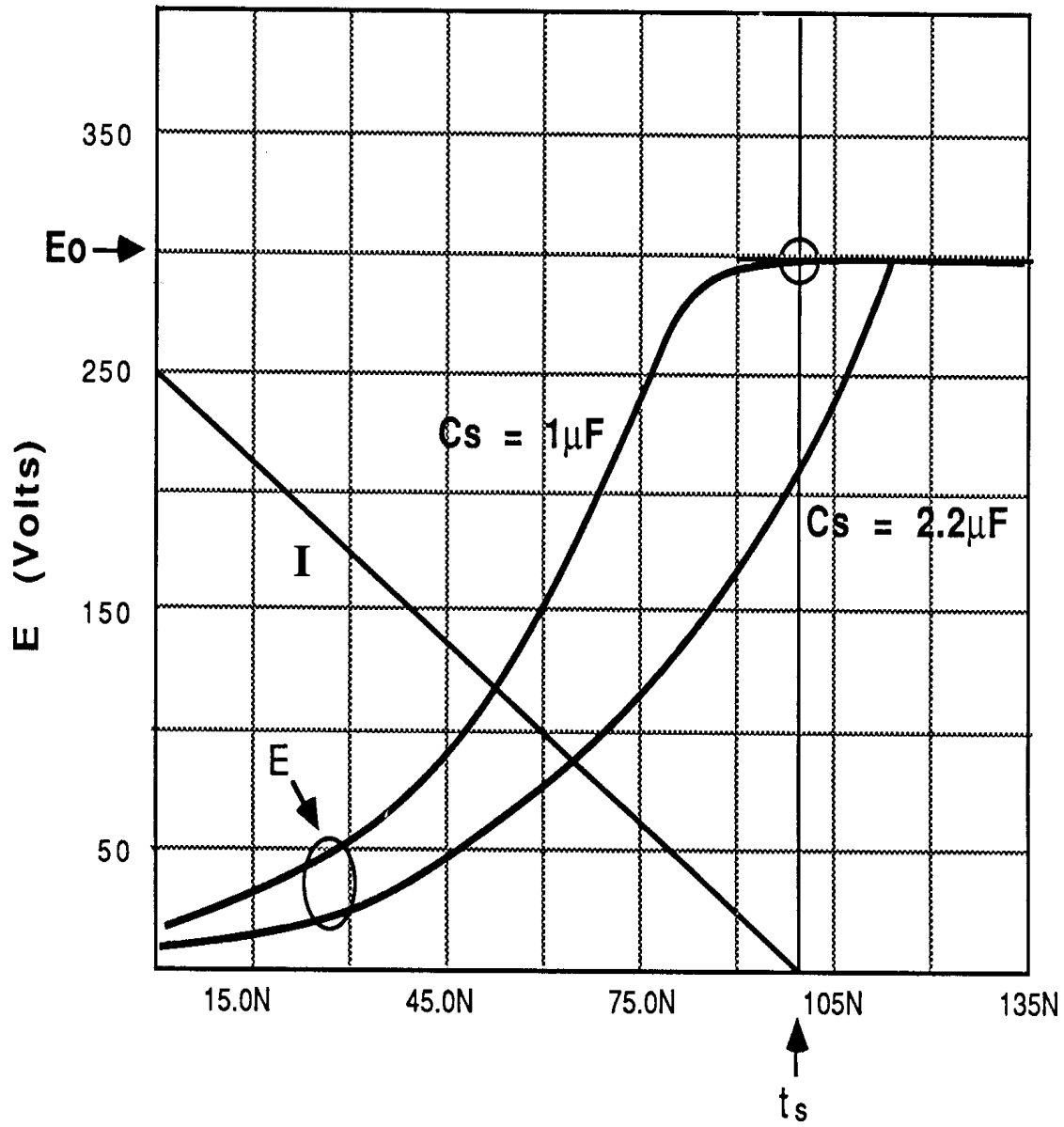
There is one disadvantage however. Because of the diode across  $R_s$ , the effective value for  $R_s$ , during the charging of  $C_s$ , is essentially zero. This is not the optimum value and, for a given  $C_s$ ,  $E_1$  will be higher than it would be in an optimized RC snubber.

Typical turn-off waveforms for this snubber are given in figure 9. These waveforms assume that  $L_p = 0$ . The effect of  $L_p$  will be considered shortly. The key feature of these waveforms is that the switch voltage rises slowly as the switch current falls. This means that the high peak power associated with

# Figure 8



# Figure 9



simultaneous maximum voltage and current is eliminated. The net result is much lower peak stress and switching loss. Voltage waveforms for two different values of  $C_s$  are shown. In this example  $I_o = 10$  A and  $E_o = 300$  V. As  $C_s$  is made larger the peak power and the switching loss will be lower. However, larger  $C_s$  means greater loss in  $R_s$  when the switch turns on and  $C_s$  is discharged through  $R_s$  and the switch. Again we see the tradeoff between snubber efficacy and loss.

Depending on the size of  $C_s$  the switch voltage may reach  $E_o$  before, at the same time, or after the switch current reaches zero. The case where  $E = E_o$  at the instant that  $I = 0$  is defined as a “normal” snubber and  $C_s = C_n$ , where<sup>[2]</sup>:

$$C = \frac{I_o t_s}{2E_o}$$

Where  $t_s$  is the fall time of the switch current (see figure 9). For the example given in figure 9,  $C_n = 1.667$  nF.

The relationships between  $C_n$ , switching loss, peak switch stress, snubber loss and total loss are shown in figure 10. Snubber size is shown relative to  $C_n$ . When even a small snubber is used ( $C_s < C_n$ ) the switching loss drops quickly. As  $C_s$  is made larger however, the improvement in switch loss decreases. For example, for  $C_s = C_n$ , the switch loss is down to 16%. Making  $C_s$  larger will reduce the switching loss only a small amount but will increase the snubber loss substantially. There is in fact a broad minimum loss around  $C_s = 0.45 C_n$ , where the total loss is reduced to 53% of what it would have been without the snubber. It is important to remember that  $C_p$  is part of  $C_s$  and that the actual value for  $C_s = .45 C_n - C_p$ . For  $C_s / C_n = 2$  the total loss is equal to what it would have been if no snubber were used, however the switching load line will have very low stress.

In those cases where the primary concern is to reduce the total switching loss, the value for  $C_s$  is usually set to  $.5 C_n$ . In this case  $R_s$  is selected to allow the voltage on  $C_s$  to decay to a small value during the minimum switch on time ( $t_{on,min}$ ). The capacitor voltage decay is a simple RC exponential and in two time constants ( $\tau = R_s C_s$ ) will be down to  $0.14 E_o$ . This is usually sufficient. The value of  $R_s$  is then:

$$R = \frac{2}{t_{on,min} C_s}$$

When  $L_p$  is significant there will be voltage overshoot during turn-off. If  $E_1$  must be controlled then different values for  $C_s$  may be necessary and a compromise made. Figure 11 gives a comparison between the RC snubber developed earlier and an RCD snubber using the same component values ( $R_s = 51\Omega$  and  $C_s = 680$  pF). Note that the loss will be lower but the peak voltage is higher for the RCD snubber. This is typical. For similar total loss,  $C_s$  can be larger in the RCD snubber which will reduce  $E_1$ . Increasing  $C_s$  to 1.2 nF reduces  $E_1$  to 424 V.  $C_s$  could be increased further but for the same total loss,  $E_1$  will still be higher in the RCD snubber.

Combined snubber: When it is important to minimize both the loss in the switch and  $E_1$

# Figure 10

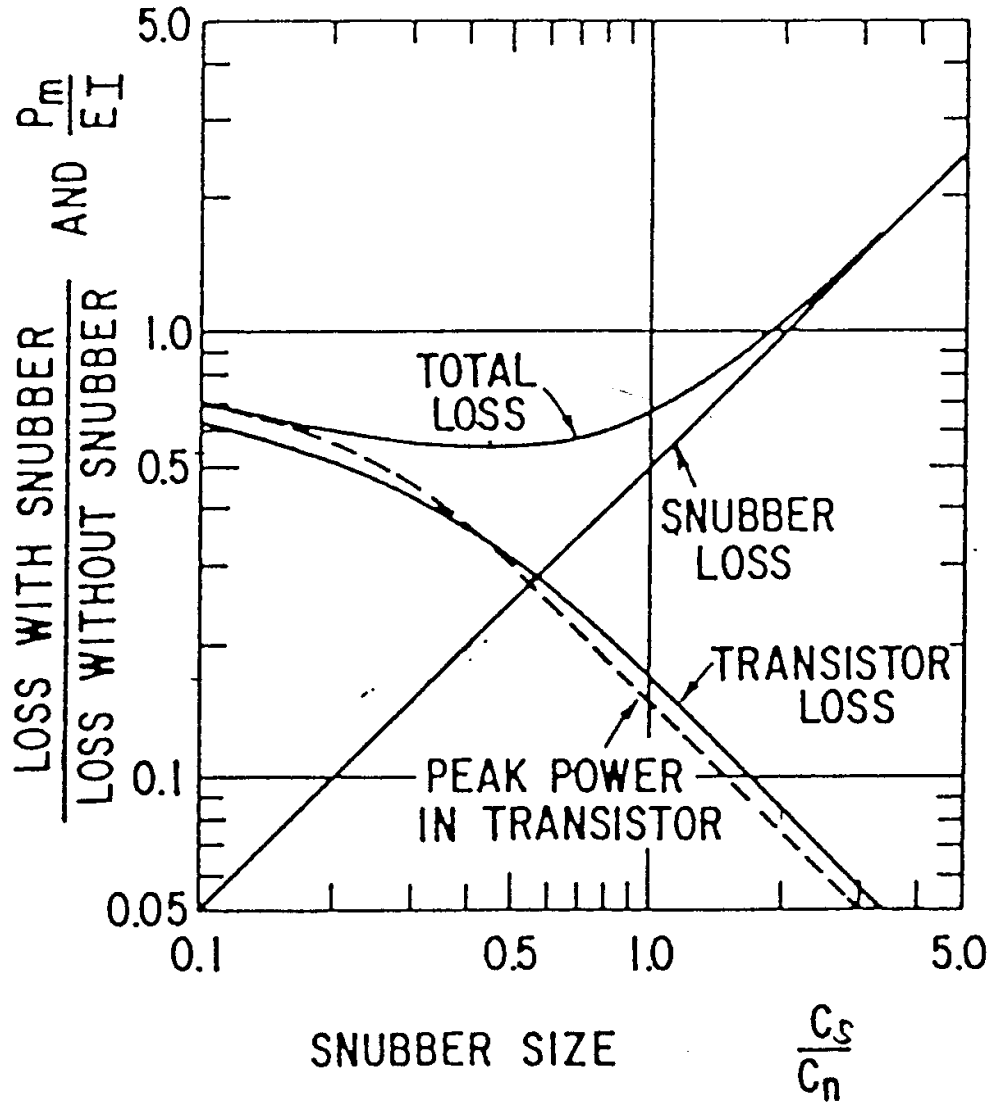
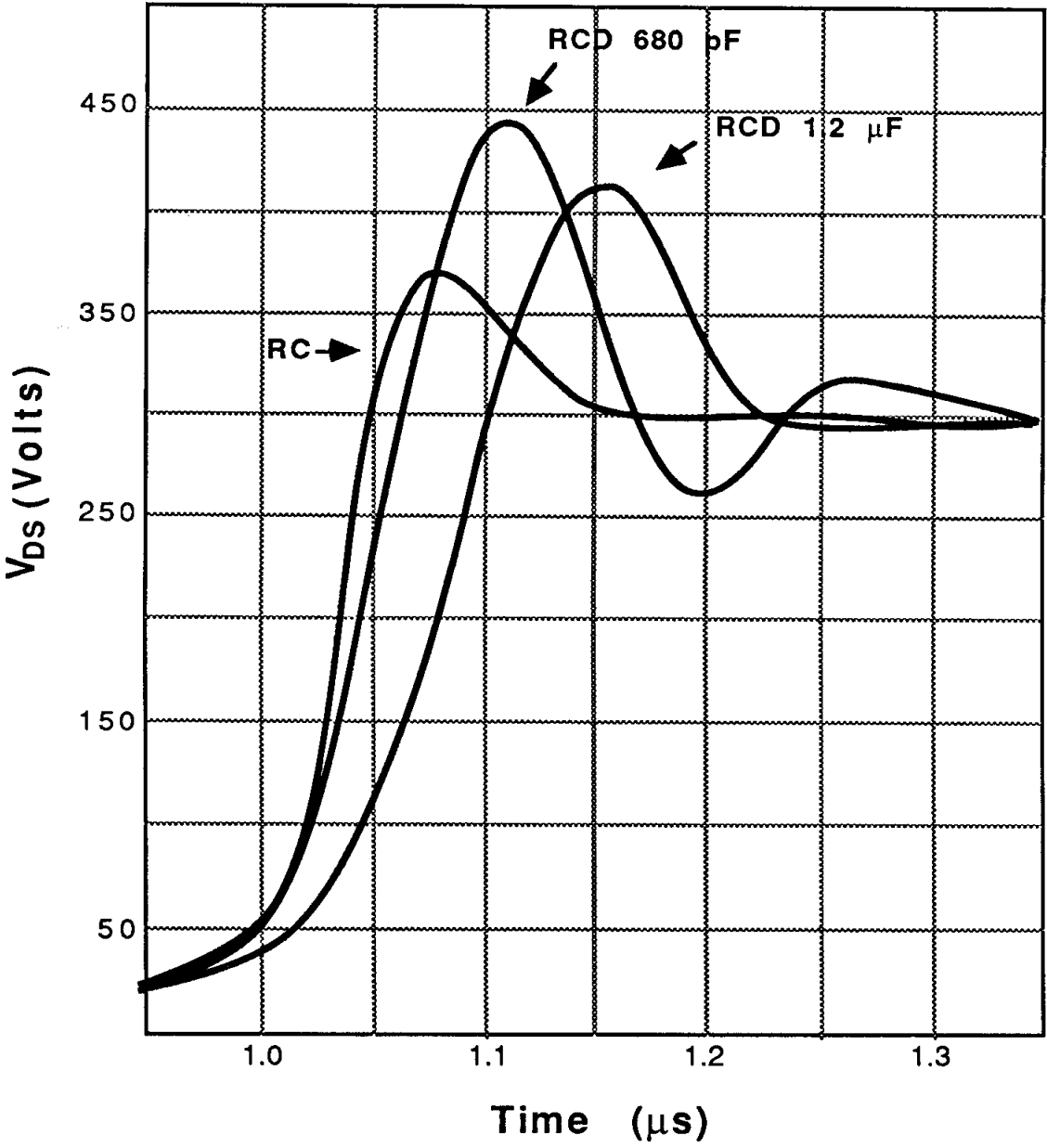




Figure 11



a combination snubber, using both RC and RCD, can produce very good results with low losses. An example of such a combination is given in figure 12 and the resulting waveform is compared to the previous RC snubber, using the same circuit conditions, in figure 13.

## Component selection and layout

The components in snubbers can be very highly stressed and must therefore be selected with some care.

### Layout and inductance

One of the primary reasons for using snubbers is the presence of parasitic inductances ( $L_p$ ) in the circuit which generate voltage spikes and ringing when excited by the switching action. Larger parasitic inductance means larger snubber components and more dissipation. Before actually designing the snubber, it is important to minimize the circuit parasitic inductances and careful circuit layout is the key. As power levels rise this becomes progressively more important because of the increasing  $dI/dt$ .

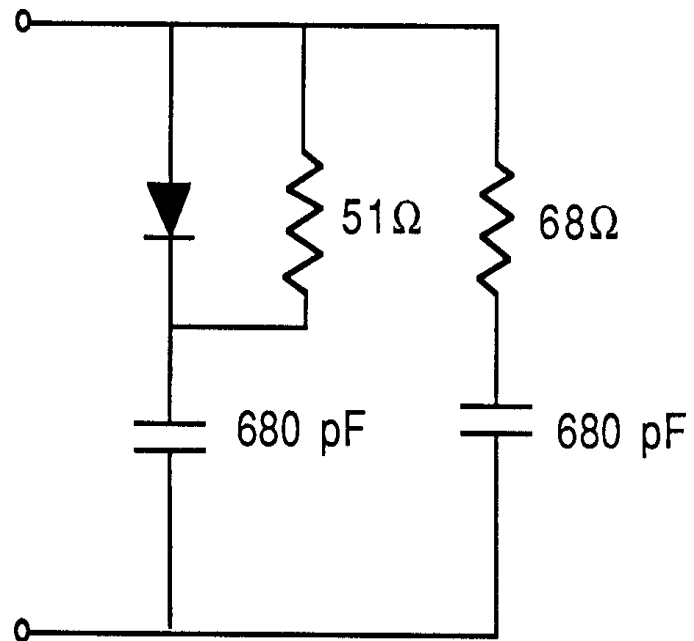
Figure 14A illustrates a typical inverter pole or converter half-bridge. The bus which connects the source ( $V_{dc}$ ) to the “+” and “-” ends of the pole will have some inherent inductance, both in the bus structure and in the energy storage capacitors ( $C_1$ , ESL). The effect of  $L_p$  can be greatly reduced by placing smaller, low ESL, capacitors as close as possible to the switches as shown by  $C_2$ . One possibility is to use CDE snubber capacitor modules which connect directly to the IGBT module as shown in figure 15. These modules are available as either a simple capacitor or they may include one or more snubber diodes to implement an RCD snubber.

In some cases the addition of  $C_2$  by itself may not be a complete answer because the bus voltage may ring due to the resonance of  $L_p$ ,  $C_1$  and  $C_2$ . An alternative is to use an RCD snubber as a clamp as shown in figure 14B. The average voltage across  $C_2$  will be equal to the bus voltage. At turn-off the voltage across  $C_2$  will rise as it limits the peak switch voltage but later in the cycle the voltage is reset to the bus voltage through  $R_s$ .  $R_s$  also damps the bus voltage ringing. An additional advantage of this approach is that  $L_p$  acts as a turn-on snubber, reducing turn-on switching loss.

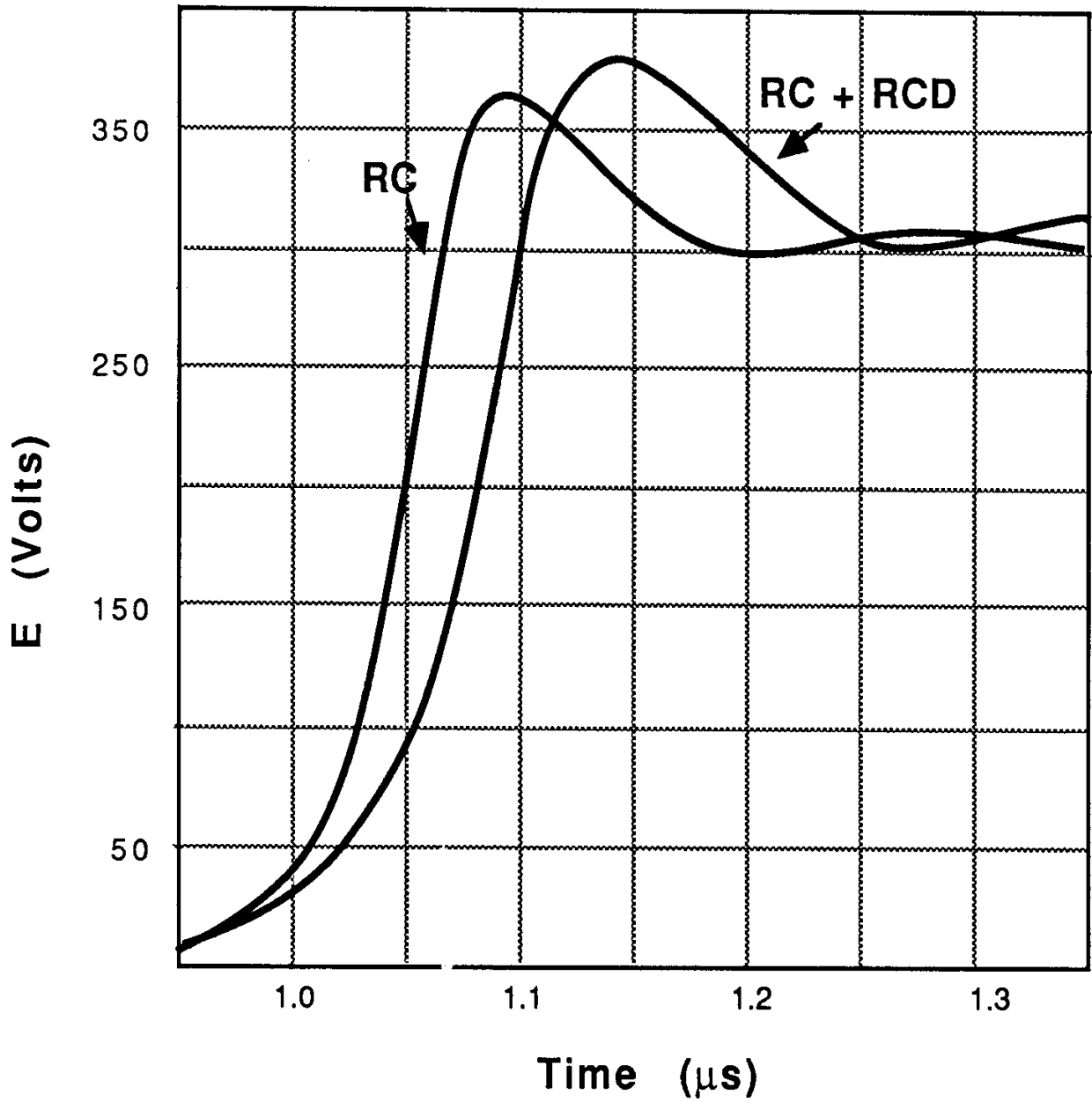
Because of the very large  $dI/dt$ 's which are common in snubbers, small amounts of parasitic inductance within the snubber can interfere with snubber action leading to higher than expected peak voltages. Parasitic inductance comes from two sources: intrinsic to the components due to physical size and lead configuration and from the layout. Component inductance can be minimized by the choice of package (radial versus axial for example) and can be further reduced by using several smaller devices in parallel. Paralleling is particularly useful in high power snubbers because in addition to allowing lower inductance configurations, it can improve the surface area-volume ratio allowing better cooling and higher rms currents.

The primary source of layout inductance is the connection from the snubber components to the switch. The snubber components should be placed as close as possible to the switch terminals. The components should be arranged so that the current

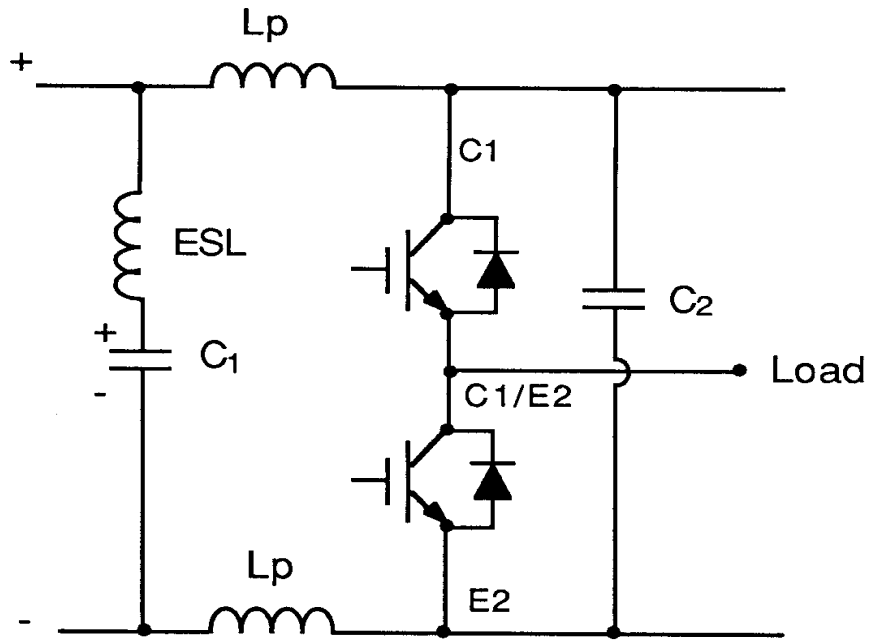
**Figure 12**



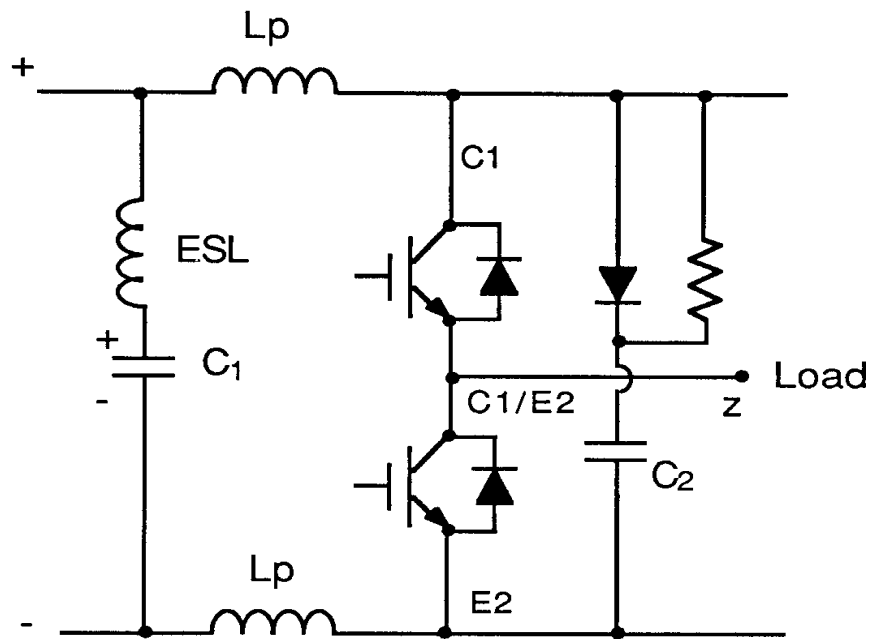
**Figure 13**



# Figure 14



(a)



(b)

loop formed by the snubber has a small an area (low inductance!) as possible. The CDE snubber modules shown in figure 15 are a very good example. With these modules, the snubber is connected directly across the switch terminals with low inductance strap leads.

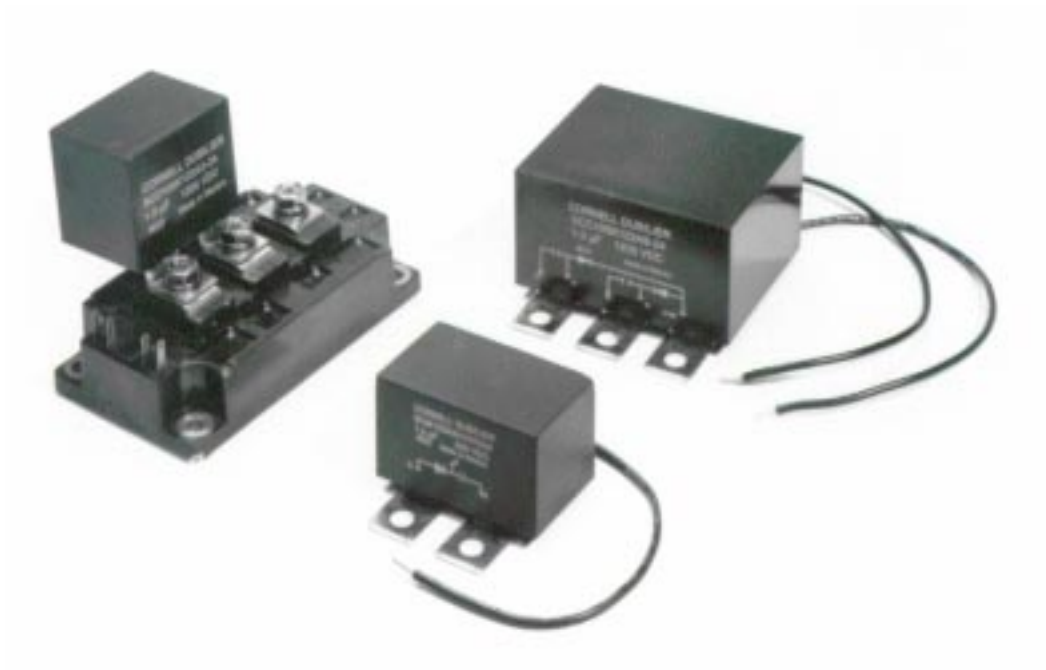
Capacitor selection: Snubber capacitors are subjected to high peak and rms currents and high dV/dt. An example of the turn-on and turn-off current spikes in a typical RCD snubber capacitor is given in figure 16. The pulses have high peak and rms amplitudes. CDE has several types of capacitors which are particularly well suited to snubber applications. Table 1 shows the various types and characteristics of capacitors intended for snubber applications.

**Table 1**  
Cornell Dubilier Capacitors for Snubber Applications

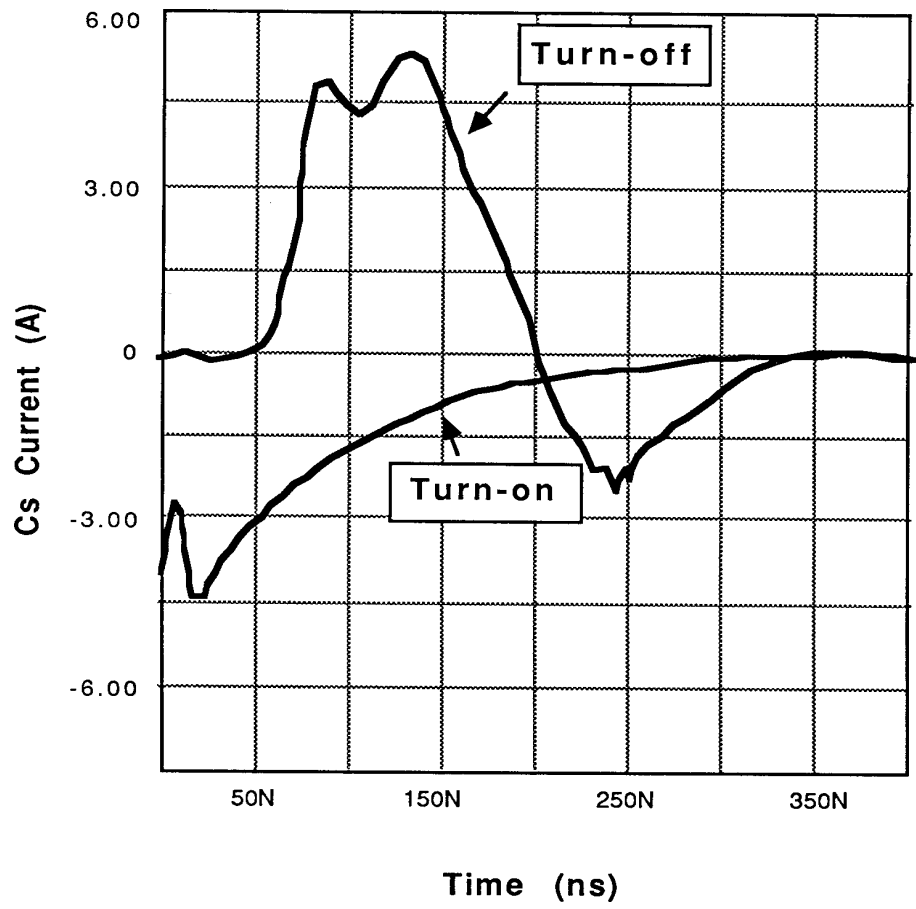
STYLE	PACKAGE	DIELECTRIC	ELECTRODE	VOLTS RANGE	CAP RANGE	dV/dt	I <sub>rms</sub>
CD16 CDV16 CDV19 CD30 CDV30	Dipped with radial leads	Mica	Foil	500-1500 VDC	100-10,000 pF	>10,000 V/μs	Up to 9 A
WPP	Wrap & Fill axial leads	Polypropylene	Foil	250-1000 VDC	0.001-2.0 μF	300-10,000 V/μs	Up to 10 A
DPF DPP	Wrap & Fill axial leads	Polypropylene	Foil	250-2000 VDC	0.01-0.47 μF	3000-10,000 V/μs	Up to 10 A
SCD	Box type, direct mount to IGBT	Polypropylene	Double Metallized	600-2000 VDC	0.1-10 μF	100-2000 V/μs	Up to 50 A
940 941	Wrap & Fill axial leads	Polypropylene	Double Metallized	600-3000 VDC	0.1-4.7 μF	100-2000 V/μs	Up to 25 A
942 943	Wrap & Fill axial leads	Polypropylene	Hybrid-metallized PP/Foil	600-2000 VDC	0.1-4.7 μF	500-5000 V/μs	Up to 25 A

Resistor selection: As pointed out earlier, it is important that  $R_s$ , in an RC snubber, have low self inductance. Inductance in  $R_s$  will increase the peak voltage ( $E_1$ ) and tend to defeat the purpose of the snubber. Low inductance is also desirable for  $R_s$  in an RCD snubber but is not as critical since the effect of a small amount of inductance is to slightly increase the reset time of  $C_s$  and reduce the peak current somewhat in the switch at turn-on. The normal choice for  $R_s$  is usually carbon composition or metal film. For higher power levels low inductance wire wound resistors, such as the Dale Electronics NH types, can be used with some care to verify the actual residual inductance and its effect on the snubber action. Again, it is in the RC snubbers that parasitic inductance is most critical.

**Figure 15**



# Figure 16





Diode selection: The diode in an RCD snubber has to be rated for at least the peak voltage which appears on  $C_s$ . In general the average current in the diode is relatively small but the peak currents are substantial. The peak current should be the basis for selecting the diode. The diode reverse recovery time ( $t_{rr}$ ) can effect the snubber action and fast or ultra-fast diodes with  $t_{rr} < 100$  ns are normally used. The performance of the diode should be verified in the circuit to be sure the snubber is performing as expected.

As the voltage rating of the diode is increased and faster recovery diodes are selected, the forward recovery time ( $t_{fr}$ ) may become a consideration. This is because the initial voltage drop across the diode, in the forward direction, can be much higher than the steady state conduction value for several hundred nsec. This problem is exacerbated by the very high  $di/dt$  of typical snubber current waveforms. By the time the diode is fully turned on, the snubber current pulse may be long finished. It may be necessary to try several different device types in the actual circuit to get satisfactory performance.

### Snubbers for IGBT inverters

IGBTs are increasingly the switch of choice for inverters used in power electronics applications. IGBTs are replacing MOSFETs in many high voltage, hard switching applications since they have lower conduction losses and smaller die area for the same output power. The smaller die size translates to lower cost and smaller input capacitance. Most IGBT modules are used in hard switching applications of up to 20 KHz. Beyond that, switching losses in the IGBT become very significant.

Switching such high currents in a short time gives rise to voltage transients that could exceed the rating of the IGBT especially if the bus voltage is close to the IGBT's voltage rating. The magnitude of the voltage transient is given by:

$$L_s \frac{di}{dt}$$

where:  $L_s$  is the 'DC loop' inductance  
 $di/dt$  is the rate of change of current with time

Design engineers are encouraged to minimize the 'DC loop' inductance. The use of laminated bus bars and improving circuit layout are ways of significantly reducing bus inductance; yet parasitic inductance will still be present. Snubbers are therefore needed to protect the switch from transients resulting from current changing in the parasitic inductance. In addition to providing protection from overvoltage, snubbers can be employed to:

- Limit  $di/dt$  or  $dV/dt$
- Shape the load line to keep it within the safe operating area (SOA)
- Transfer power dissipation from the switch to a resistor
- Reduce total switching losses
- Reduce voltage and current ringing

There are three basic types of snubbers circuits used in IGBT applications. The type used will depend largely on the power level, switching frequency, and circuit layout. Figure 18 shows these snubber circuits and how they are applied to a half bridge rectifier.

The de-coupling is the simplest of the three types. It is essentially a low inductance capacitor mounted across the bus, from C to E on a dual IGBT module, or from P to N on a six pack. The de-coupling is effective in reducing transients by providing a low inductance path during switching operation. De-coupling caps are typically used in low to medium current applications. In higher current applications, oscillations between the source and the de-coupling capacitor will produce ripple current that may cause the capacitor to fail.

Cornell Dubilier offers 940, 941, and SCD (Direct mount) capacitors for de-coupling applications. The 940 series capacitors are axial leaded and can be mounted onto a PCB while style SCD caps are mounted directly to the IGBT module. Direct mount types have lower inductance due to the flat, radial lead geometry. They are easy to install using the IGBT's own screws. Direct mount capacitors are rated for higher current because heavy copper lugs are connected directly to the capacitor element.

The value of the capacitance needed for a de-coupling application depends on the stray inductance, maximum switching current, allowable peak voltage and dc bus voltage. The Snubber capacitance needed can be approximated from the following:<sup>16</sup>

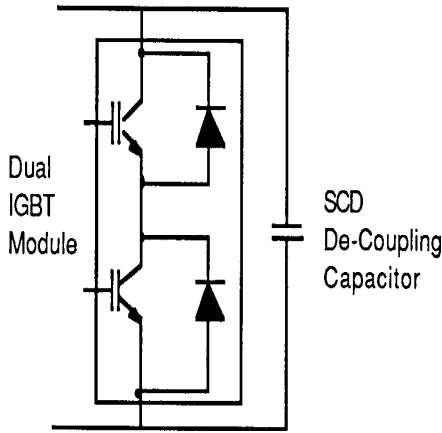
$$C_s = \frac{LsI_o^2}{(V_{pk} - V_{cc})}$$

The difficulty in applying this formula is that bus inductance is often difficult to determine. Pages 10 through 12 of this application note provide a couple of methods for determining L. A good rule of thumb is to use 1  $\mu$ F per 100 A of IGBT if inductance cannot be determined directly.

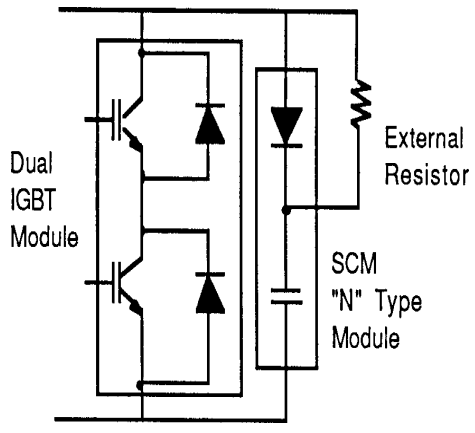
RCD snubbers are typically used in medium to high current applications. Direct mount snubbers containing hyperfast, soft recovery diodes are available from Cornell Dubilier. Style SCM may be used to protect dual IGBT modules by connecting them across the C and E terminals of the IGBT. See figure 18B. This snubber operates on the same principles as the de-coupling capacitor, but only during turn-off switching. As the IGBT turns off, energy trapped in the loop inductance is transferred to the capacitor. The diode blocks oscillations and the excess charge on the capacitor is dissipated through the external resistor.

In higher current applications where the inverter is made of two single IGBT modules, "P" type and "N" type SCM snubbers may be applied to clamp the inverter voltage as shown in figure 18C. Dual IGBT modules may also be protected using an SCC style "clamp" module as shown in figure 18D. At turn off, the snubber diode is forward biased and the snubber is activated. The energy trapped in the stray inductance is absorbed by the snubber capacitor. During turn-on the snubber caps that were fully charged to bus voltage have a discharge path through the forward bias free-wheel diode, the IGBT, and the snubber resistor. This reduces the reverse recovery voltage transient.

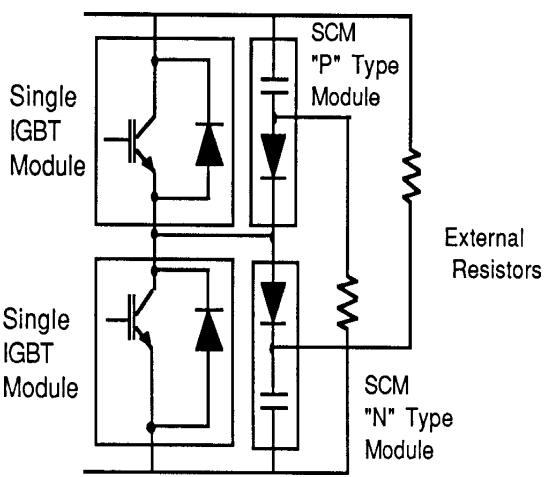
# Figure 18



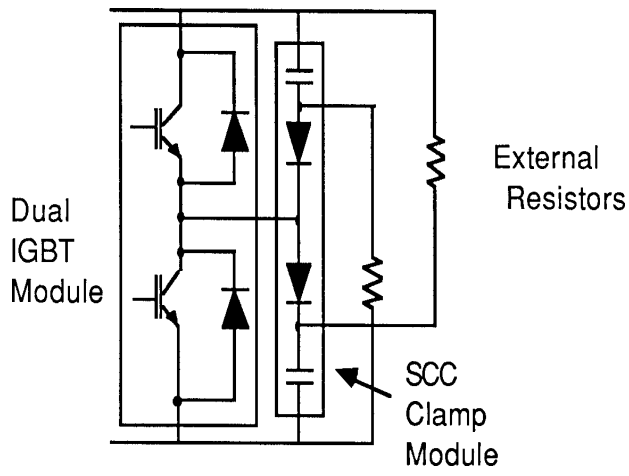
a



b



c



d

As the need for high power snubbers continues to increase, so does the need for information regarding appropriate component selection. This paper discussed the major types of snubbers, their application and methods for determining snubber component values. Use of these methods should lead to good component choice and ultimately good snubber design.

## References

- [1] William McMurray, OPTIMUM SNUBBERS FOR POWER SEMICONDUCTORS, IEEE IAS transactions, Vol. IA-8, No. 5, Sept/Oct 1972, pp. 593-600
- [2] William McMurray, SELECTION OF SNUBBERS AND CLAMPS TO OPTIMIZE THE DESIGN OF TRANSISTOR SWITCHING CONVERTERS, IEEE IAS transactions, Vol. IA-16, No. 4, July/August 1980, pp. 513-523
- [3] Motto, E., EVALUATING THE DYNAMIC PERFORMANCE OF HIGH CURRENT IGBT MODULES
- [4] Kurnia, Stielau, Venkataramanan and Divan, LOSS MECHANISMS IN IGBT'S UNDER ZERO VOLTAGE SWITCHING, IEEE APEC 92 proceedings, pp. 1011-1017
- [5] Wang, Lee, Hua and Borjovic, A COMPARATIVE STUDY OF SWITCHING LOSSES OF IGBT'S UNDER HARD-SWITCHING, ZERO-VOLTAGE-SWITCHING AND ZERO-CURRENT-SWITCHING, IEEE PESC 94 proceedings, pp. 1196-1204
- [6] Johansen, Jensen and Rogne, CHARACTERIZATION OF HIGH POWER IGBT'S WITH SINEWAVE CURRENT, IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, VOL. 30, No. 5, September/October 1994, pp. 1142-1147
- [7] Udeland, T., SWITCHING STRESS REDUCTION IN POWER TRANSISTOR CONVERTERS, IEEE IAS annual meeting proceedings, 1976, pp. 383-392
- [8] Domb, M., NONDISSIPATIVE TURN-OFF SNUBBER ALLEVIATES SWITCHING POWER DISSIPATION, SECOND-BREAKDOWN STRESS AND  $V_{CE}$  OVERSHOOT, IEEE PESC proceedings, 1982, pp. 445-454
- [9] Zach, Kaiser, Kolar and Haselsteiner, NEW LOSSLESS TURN-ON AND TURN-OFF (SNUBBER) NETWORKS FOR INVERTERS, INCLUDING CIRCUITS FOR BLOCKING VOLTAGE LIMITATION, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. PE-1, NO. 2, April 1986, pp. 65-75

- [10] Bendien, Van Der Broeck and Fregien, RECOVERY CIRCUIT FOR SNUBBER ENERGY IN POWER ELECTRONIC APPLICATIONS WITH HIGH SWITCHING FREQUENCIES, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 3, NO. 1, January 1988, pp. 26-30
- [11] Simonelli, and Torrey, AN ALTERNATIVE BUS CLAMP FOR RESONANT DC-LINK CONVERTERS, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 9, NO. 1, January 1994, pp. 56-63
- [12] Finney, Williams and Green, RCD SNUBBER REVISITED, IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, VOL. 32, NO. 1, January 1996, pp. 155-160
- [13] McMurray, W., EFFICIENT SNUBBERS FOR VOLTAGE-SOURCE INVERTERS, IEEE PESC 85 proceedings, 1985, pp. 20-27
- [14] Swanepoel and van Wyk, ANALYSIS AND OPTIMIZATION OF REGENERATIVE LINEAR SNUBBERS APPLIED TO SWITCHES WITH VOLTAGE AND CURRENT TAILS, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 9, NO. 4, July 1994, pp. 433-441
- [15] Pearson and Sen, DESIGNING OPTIMUM SNUBBER CIRCUITS FOR THE TRANSISTOR BRIDGE CONFIGURATION, POWERCON 9 proceedings, 1982, pp. D-2-1 through D-2-11
- [16] Zhang, Sobhani and Chokhawala, SNUBBER CONSIDERATIONS FOR IGBT APPLICATIONS, INTERNATIONAL RECTIFIER DESIGNER'S MANUAL, IGBT-3, TPAP-5, 1995, pp. E135-E144.